IN THE CLAIM:

Please amended claims 2, 4 and 6 as follows:

1. (Canceled).

2. (Currently Amended) A shared memory multiprocessor comprising:

a plurality of nodes each configured with at least one of a processor having a cache memory, a memory device and an I/O device; and

an inter-node connection network for interconnecting a plurality of said nodes;

wherein at least one of a plurality of said nodes includes at least two of said processor, ~~and~~ said memory device and said I/O device, and the ~~whole of a~~ plurality of said nodes include at least one said processor, at least one said memory device and at least one said I/O device[[;]],

wherein each of said nodes includes

an information adding unit for adding, to a memory access request or an I/O access request issued by said processor or said I/O device in [[the]] a respective local node, node information indicating a node constituting a destination of transfer of the access request, and

a transfer unit for selectively transferring the access request to said inter-node connection network in accordance with the node information added to the access request[[;]], and

wherein said inter-node connection network transfers said access request to the node indicated by the node information added to said access request.

3. (Original) A shared memory multiprocessor according to claim 2, wherein said inter-node connection network is a crossbar switch.

4. (Currently Amended) A shared memory multiprocessor comprising:

a plurality of nodes each configured with at least one of a processor having a cache memory, a memory device and an I/O device; and

an inter-node connection network for interconnecting a plurality of said nodes;

wherein at least one of a plurality of said nodes includes at least two of said processor, ~~and~~ said memory device and said I/O device, and the ~~whole of a~~ plurality

of said nodes include at least one said processor, at least one said memory device and at least one said I/O device;

wherein each of said nodes includes

an access request analysis unit for analyzing a memory access request or an I/O access request issued by said processor or said I/O device in [[the]] a respective local node to determine whether or not cache coherence control is required or to check node information indicating a node constituting a destination of transfer of the access request, and

a transfer unit for selectively transferring the access request to said inter-node connection network in accordance with a result of the analysis, and

wherein when it is determined that the cache coherence control is required, said access request is broadcasted to all ~~the~~ nodes requiring the cache coherence control among a plurality of said nodes through said inter-node connection network,

when said access request indicates an access to another one of a plurality of said nodes and it is determined that the cache coherence control is not required, said access request is directly transferred only to the another node indicated by the node information through said inter-node connection network, and

when said access request indicates an access to the local node and it is determined that the cache coherence control is not required, said access request is not outputted to said inter-node connection network.

5. (Original) A node controller shared memory multiprocessor according to claim 4, wherein said inter-node connection network is a crossbar switch.

6. (Currently Amended) A node controller included in each node of a shared memory multiprocessor comprising:

a plurality of nodes each configured with at least one of a processor having a cache memory, a memory device and an I/O device; and

an inter-node connection network for interconnecting a plurality of said nodes,

wherein at least one of a plurality of said nodes includes at least two of said processor, ~~and~~ said memory device and said I/O device, and the ~~whole of a~~ plurality of said nodes include at least one said processor, at least one said memory device and at least one said I/O device;

wherein said node controller includes

an access request analysis unit for analyzing a memory access request or an I/O access request issued by said processor or said I/O device in [[the]] a respective local node, and

a transfer unit for selectively transferring the access request to said inter-node connection network in accordance with a result of the analysis.